

CLAIMS

1 1. (currently amended) A programmable logic device (PLD), comprising a logic core
2 connected to an input/output (I/O) interface, the I/O interface comprising one or more programmable I/O
3 buffers (PIBs), wherein:

4 at least one PIB can be programmed to perform ~~two~~ three or more of:

5 (a) a double data rate (DDR) input mode in which an incoming DDR data signal is
6 converted into two single data rate (SDR) data signals that are made available to the logic core;

7 (b) one or more demux input modes, different from the DDR input mode, in which
8 an incoming data signal is demultiplexed into two or more lower-rate data signals that are made available
9 to the logic core;

10 (c) one or more DDR demux input modes in which an incoming DDR data signal is
11 converted into four or more lower-rate SDR data signals that are made available to the logic core; and

12 (d) one or more additional input modes in which an incoming data signal is made
13 available to the logic core without any demultiplexing or DDR-to-SDR conversion; and

14 the at least one PIB can be programmed to perform ~~two~~ three or more of:

15 (a) a DDR output mode in which two SDR data signals from the logic core are
16 converted into a single outgoing DDR data signal;

17 (b) one or more mux output modes, different from the DDR output mode, in which
18 two or more data signals from the logic core are multiplexed into a single, higher-rate, outgoing data
19 signal;

20 (c) one or more DDR mux output modes in which four or more SDR data signals
21 from the logic core are converted into a single, higher-rate, outgoing DDR data signal; and

22 (d) one or more additional output modes in which a data signal from the logic core is
23 provided as an outgoing data signal without any multiplexing or SDR-to-DDR conversion.

1 2. (original) The invention of claim 1, wherein the PLD is a field programmable gate array
2 (FPGA).

1 3. (original) The invention of claim 1, wherein:

2 the one or more additional input modes comprise a pass-through data input mode and an input
3 register mode; and

4 the one or more additional output modes comprise a pass-through data output mode and an
5 output register mode.

1 4. (original) The invention of claim 1, wherein, during each DDR demux input mode:

2 the incoming DDR data signal is converted into first and second SDR data signals;

3 the first SDR data signal is demultiplexed into a first set of two or more lower-rate SDR data
4 signals; and

5 the second SDR data signal is demultiplexed into a second set of two or more lower-rate SDR
6 data signals.

1 5. (original) The invention of claim 1, wherein, during each DDR mux output mode:

2 a first set of two or more SDR data signals are multiplexed into a first higher-rate SDR data
3 signal;

4 a second set of two or more SDR data signals are multiplexed into a second higher-rate SDR data
5 signal; and

6 the first and second SDR data signals are converted into the outgoing DDR data signal.

1 6. (currently amended) The invention of claim 1, wherein the PIB supports a plurality of
2 different demux input modes having different levels of demuxing, a plurality of different DDR demux
3 input modes having different levels of demuxing, a plurality of different mux output modes having
4 different levels of muxing, and a plurality of different DDR mux output modes having different levels of
5 muxing.

1 7. (original) The invention of claim 6, wherein:
2 the plurality of demux input modes includes (1:1), (1:2), and (1:4) levels of demuxing;
3 the plurality of DDR demux input modes includes (1:1), (1:2), and (1:4) levels of demuxing, each
4 combined with DDR-to-SDR conversion;
5 the plurality of mux output modes includes (1:1), (2:1), and (4:1) levels of muxing; and
6 the plurality of DDR mux output modes includes (1:1), (2:1), and (4:1) levels of muxing, each
7 combined with SDR-to-DDR conversion.

1 8. (original) The invention of claim 1, wherein, to support the input modes, the PIB
2 comprises:
3 (1) a DDR stage adapted to convert an incoming DDR data signal into two SDR data signals;
4 and
5 (2) a shift stage and an update stage adapted to demultiplex one or more data signals into
6 two or more lower-rate data signals.

1 9. (original) The invention of claim 8, wherein:
2 the DDR stage comprises two flip-flops (FFs), each adapted to receive the incoming DDR data
3 signal and generate a different one of the two SDR data signals;
4 the shift stage comprises two sets of one or more FFs, each set configured as a shift register; and
5 the update stage comprises a set of one or more FFs corresponding to each shift register of the
6 shift stage.

1 10. (original) The invention of claim 8, wherein the PIB further comprises a transfer stage
2 adapted to apply a time-domain transfer to one or more data signals.

1 11. (original) The invention of claim 10, wherein the DDR, shift, and update stages are
2 adapted to be driven by a first clock signal, and the transfer stage is adapted to be driven by a second
3 clock signal, corresponding to the time domain of the logic core.

1 12. (original) The invention of claim 1, wherein, to support the output modes, the PIB
2 comprises:
3 (1) one or more shift registers adapted to multiplex two or more data signals to generate at least
4 one higher-rate data signal; and
5 (2) a mux adapted to convert two SDR data signals into a single DDR data signal.

1 13. (original) The invention of claim 12, wherein the PIB further comprises a transfer stage
2 adapted to apply a time-domain transfer to one or more data signals.

1 14. (original) The invention of claim 13, wherein the shift registers and the mux are adapted
2 to be driven by a first clock signal, and the transfer stage is adapted to be driven by a second clock signal
3 corresponding to the time domain of the logic core.

1 15. (currently amended) A programmable logic device (PLD), comprising a logic core
2 connected to an I/O interface, the I/O interface comprising one or more programmable I/O buffers (PIBs),
3 wherein at least one PIB can be programmed to perform ~~two~~ three or more of:

4 (a) a double data rate (DDR) input mode in which an incoming DDR data signal is converted
5 into two single data rate (SDR) data signals that are made available to the logic core;
6 (b) a demux input mode, different from the DDR input mode, in which an incoming data
7 signal is demultiplexed into two or more lower-rate data signals that are made available to the logic core;
8 (c) a DDR demux input mode in which an incoming DDR data signal is converted into four
9 or more lower-rate SDR data signals that are made available to the logic core; and
10 (d) one or more additional input modes in which an incoming data signal is made available
11 to the logic core without any demultiplexing or DDR-to-SDR conversion.

1 16. (currently amended) A programmable logic device (PLD), comprising a logic core
2 connected to an I/O interface, the I/O interface comprising one or more programmable I/O buffers (PIBs),
3 wherein at least one PIB can be programmed to perform ~~two~~ three or more of:

4 (a) a DDR output mode in which two SDR data signals from the logic core are converted
5 into a single outgoing DDR data signal;
6 (b) a mux output mode, different from the DDR output mode, in which two or more data
7 signals from the logic core are multiplexed into a single, higher-rate, outgoing data signal;
8 (c) a DDR mux output mode in which four or more SDR data signals from the logic core are
9 converted into a single, higher-rate, outgoing DDR data signal; and
10 (d) one or more additional output modes in which a data signal from the logic core is
11 provided as an outgoing data signal without any multiplexing or SDR-to-DDR conversion.

1 17. (currently amended) A programmable logic device (PLD), comprising a logic core
2 connected to an I/O interface, the I/O interface comprising one or more programmable I/O buffers (PIBs),
3 wherein at least one PIB comprises a transfer stage adapted to apply a time-domain transfer to one or
4 more data signals, wherein the transfer stage is adapted to be driven by a system clock signal
5 corresponding to the time domain of the logic core.

1 18. (currently amended) The invention of claim 17, wherein the transfer stage is adapted to
2 be driven by a system clock signal, corresponding to the time domain of forms an interface between the
3 logic core and additional circuitry within the at least one PIB.

1 19. (currently amended) The invention of claim 18, wherein the additional circuitry within
2 the at least one PIB is adapted to be driven by another clock signal different from the system clock signal
3 not corresponding to the time domain of the logic core.

1 20. (original) A programmable logic device (PLD), comprising a logic core connected to an
2 I/O interface, the I/O interface comprising one or more programmable I/O buffers (PIBs), wherein at least
3 one PIB comprises:

4 double data rate (DDR) circuitry programmable to convert an incoming DDR data signal into two
5 single data rate (SDR) data signals; and
6 demultiplexing circuitry coupled to the DDR circuitry and programmable to demultiplex each of
7 the two SDR data signals into two or more lower-rate SDR data signals.

1 21. (original) A programmable logic device (PLD), comprising a logic core connected to an
2 I/O interface, the I/O interface comprising one or more programmable I/O buffers (PIBs), wherein at least
3 one PIB comprises:

4 multiplexing circuitry programmable to multiplex four or more outgoing single data rate (SDR)
5 data signals into two higher-rate SDR data signals; and
6 double data rate (DDR) circuitry coupled to the multiplexing circuitry and programmable to
7 convert the two higher-rate SDR data signals into an outgoing DDR data signal.